

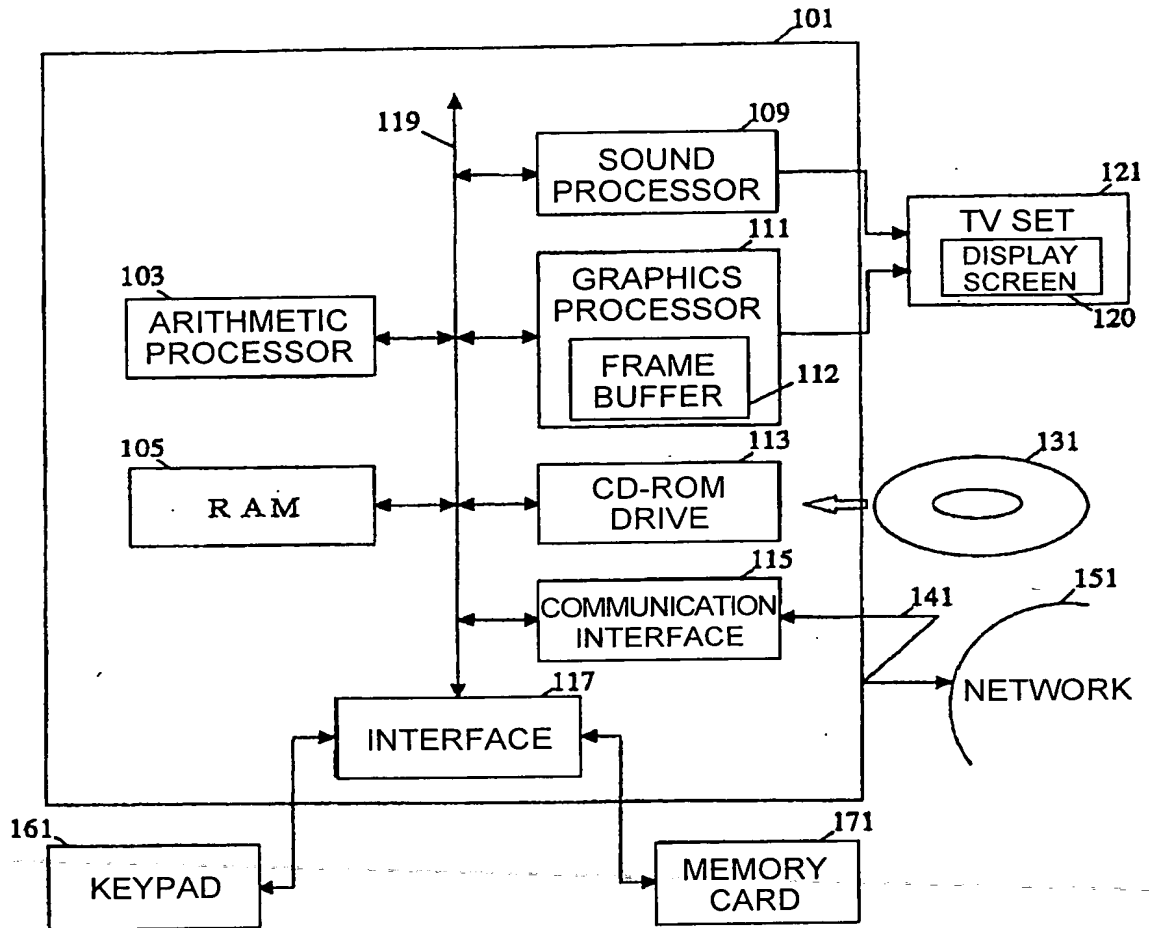
Fig.1

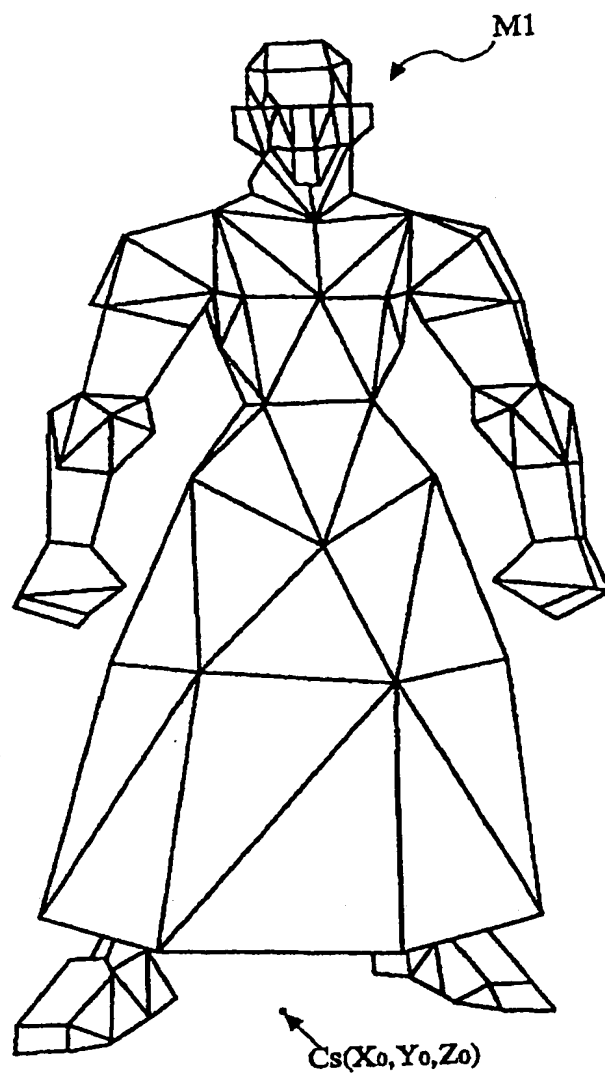
Fig.3

1054

541 OBJECT ID No.	543 POLYGON ID No.	545 VERTEX ID No.
M1	P1	V1
		V2
		V3
	P2	V3
		V2
		V4
	P3	V4
		V5
		V3
	⋮	⋮
⋮	⋮	⋮

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09634316316300



1056

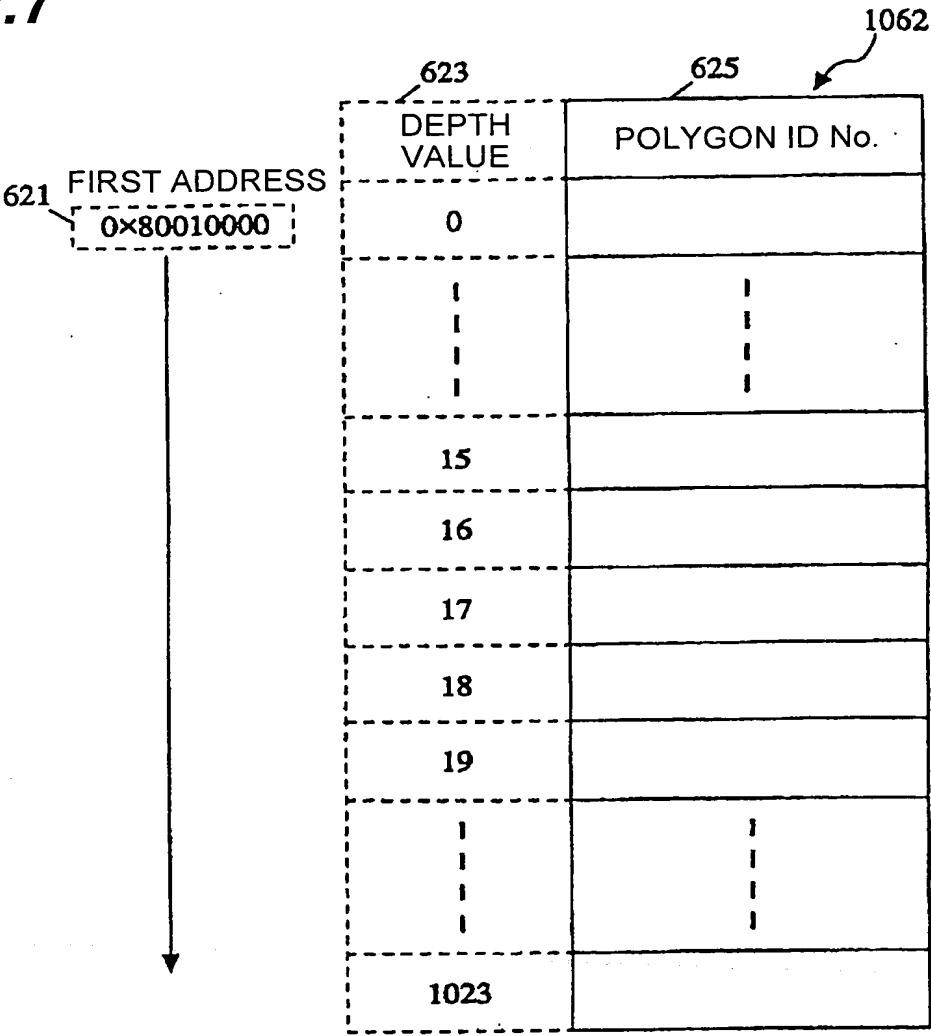
561

1058

581

OBJECT ID No.	LIGHTNESS ADJUSTMENT VALUES	COORDINATE ADJUSTMENT VALUES	DEPTH ADJUSTMENT VALUES
M1	Rd,Gd,Bd	(Xd,Yd,Zd)	Dd
M3	Re,Gc,Be	(Xe,Yc,Zc)	De
M8	Rf,Gf,Bf	(Xf,Yf,Zf)	Df
⋮	⋮	⋮	⋮

Fig.7



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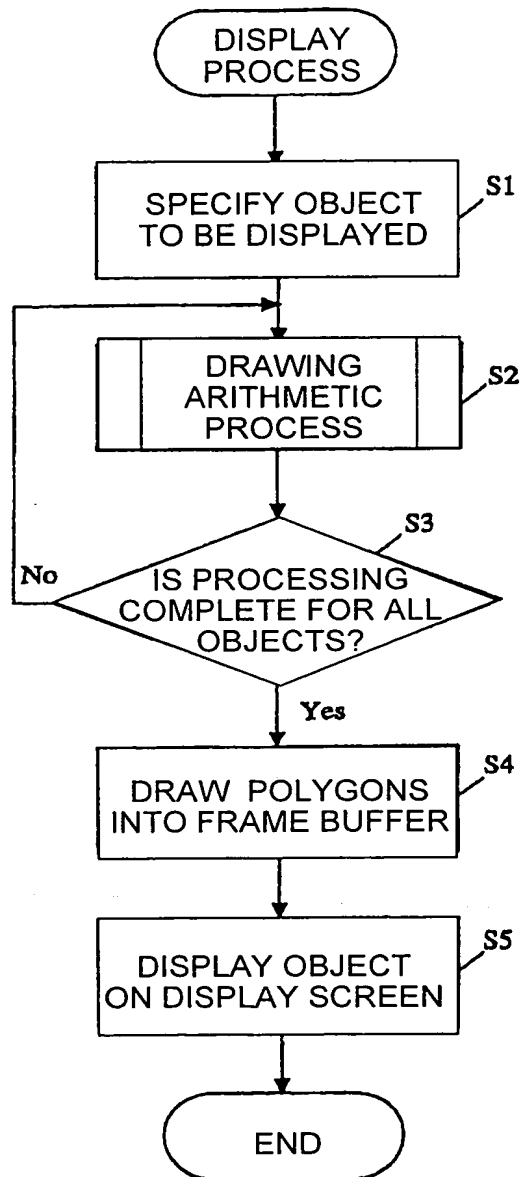
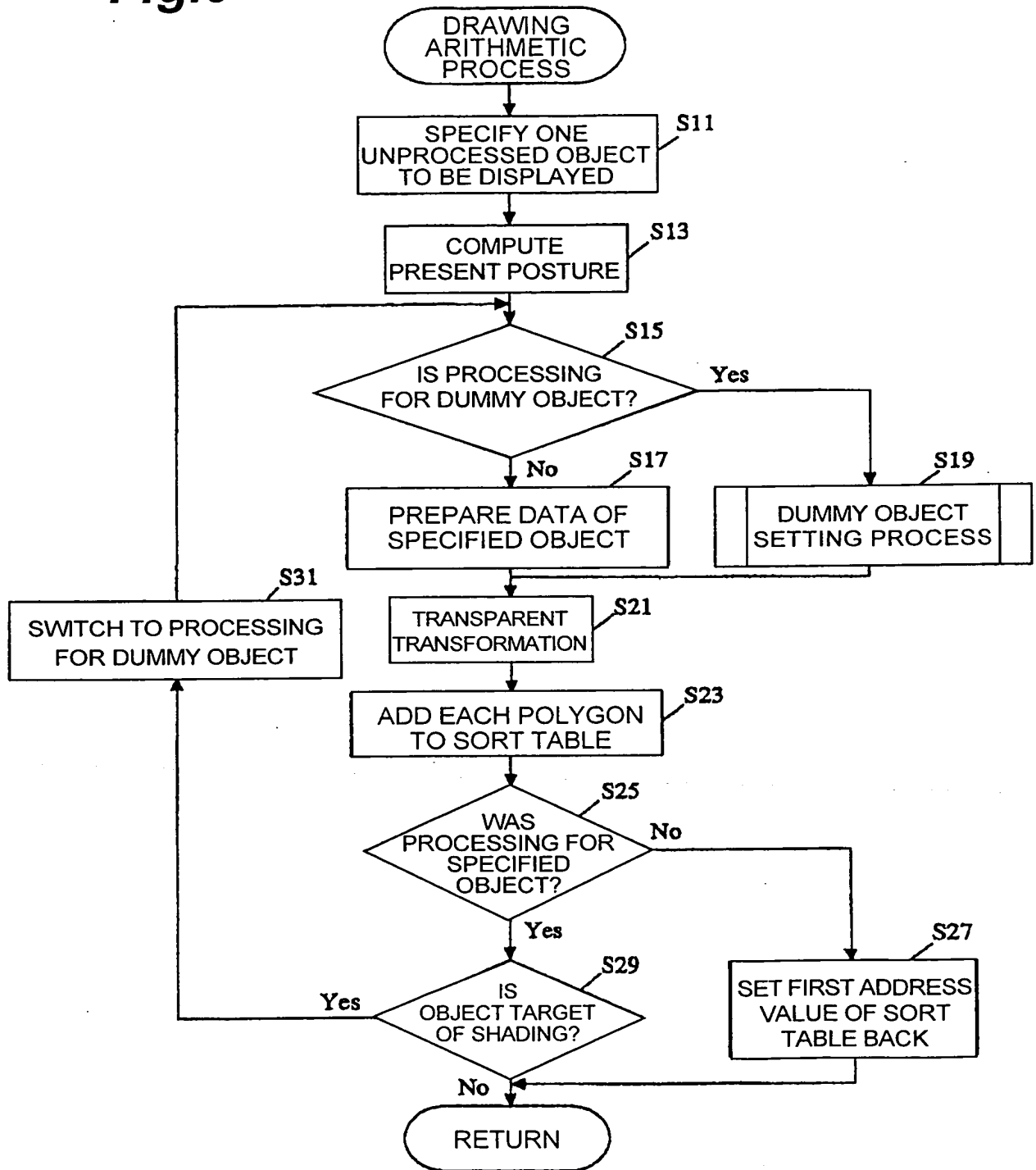
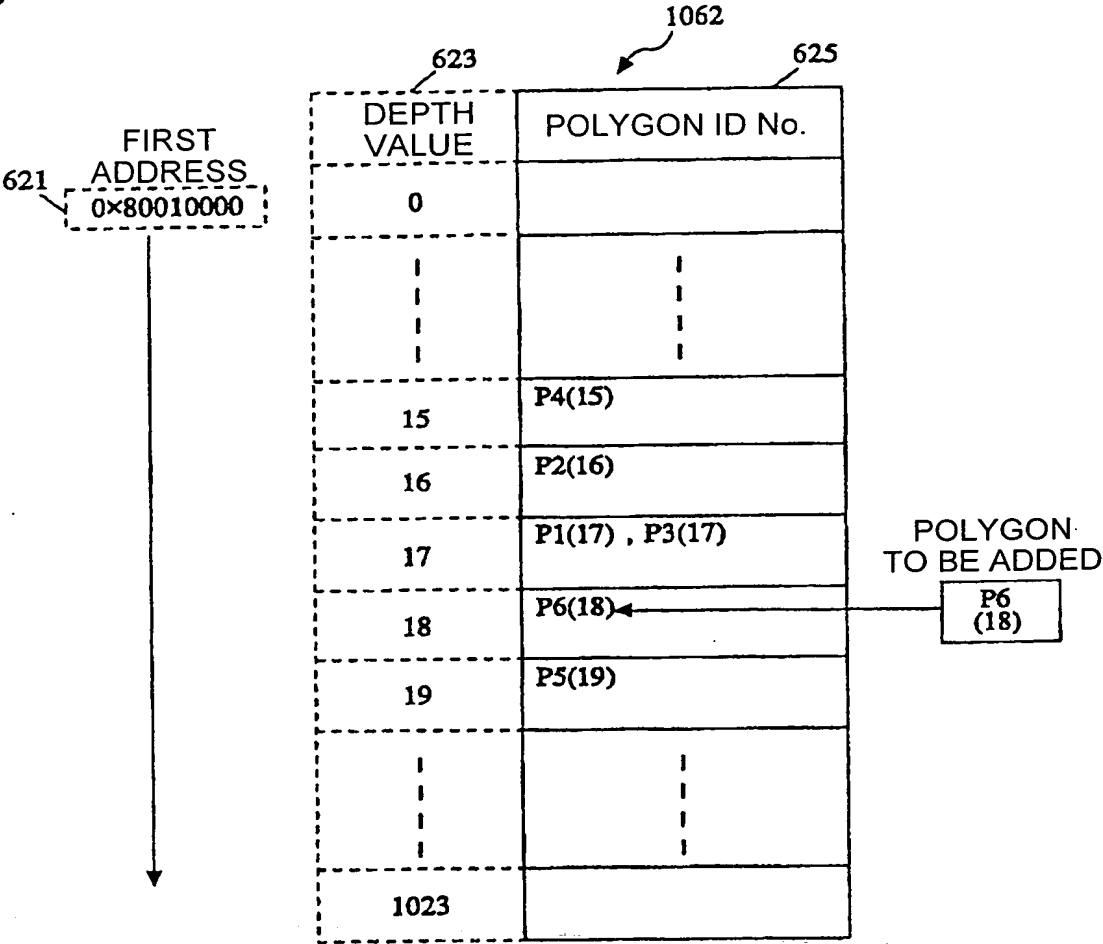
Fig.8

Fig.9



00751393 122700

Fig.10



00/22T" E6ET5/60

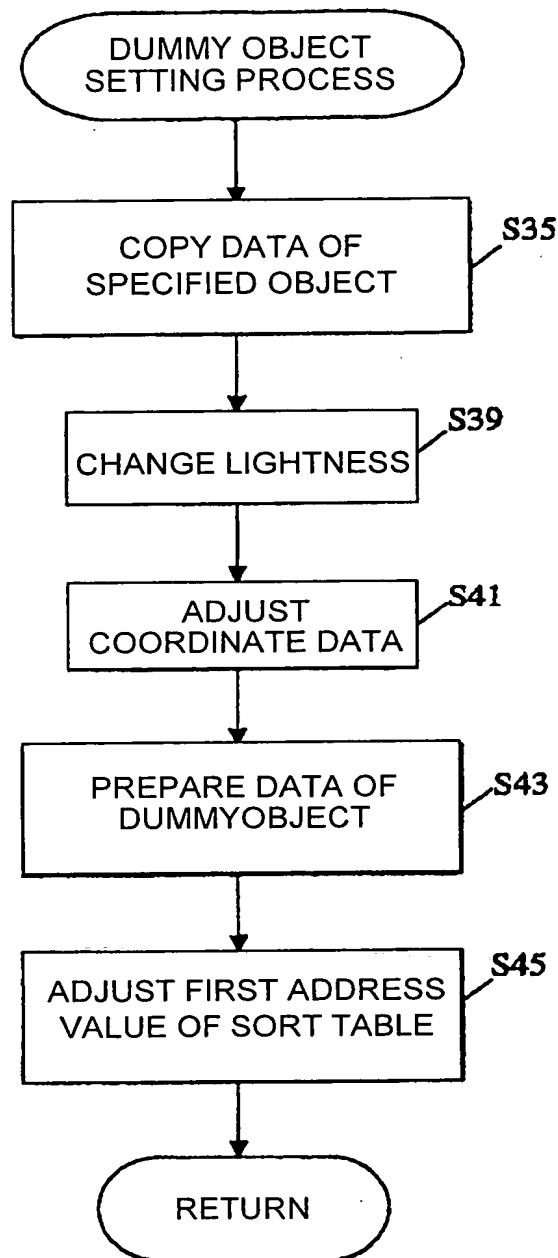
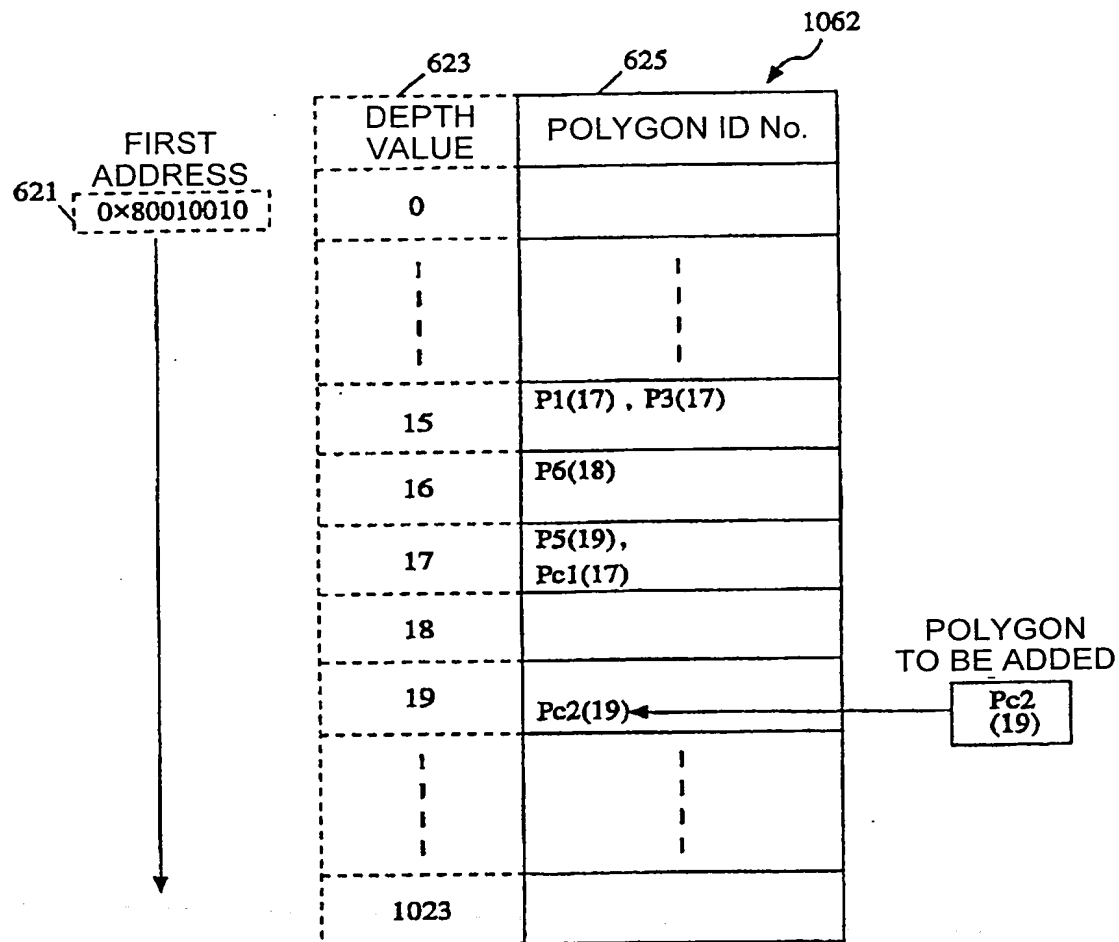
Fig.11

Fig.12



00422T" E6ET5/60

Fig.13

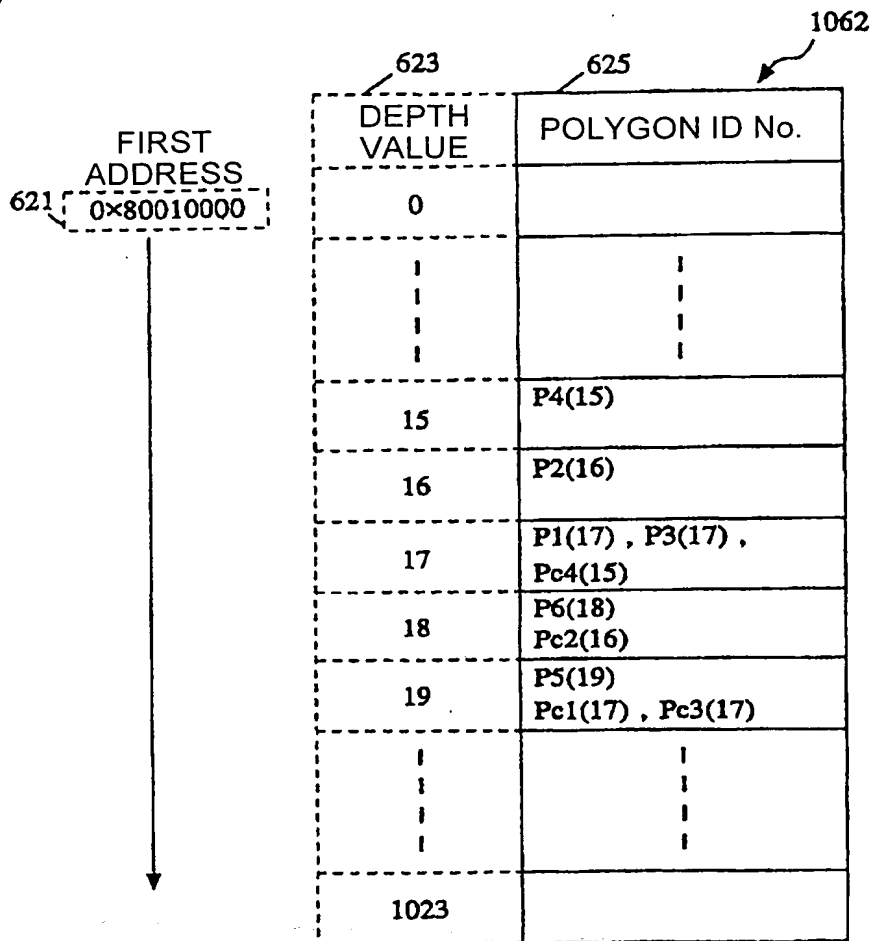


Fig.15

641 PIXEL ID No.	643 1064 COLOR DATA (R,G,B)
1	
2	
3	
1 1 1 1	1 1 1 1

Fig.16

Fig. 16 is a schematic diagram of a memory array 120. The array is organized into rows and columns. The first row is labeled with indices 0, 1, 2, followed by four dashes, and then 318, 319. The second row is labeled with indices 320, 321, 322, followed by four dashes, and then 638, 639. The array is enclosed in a large bracket on the left labeled 240 and a large bracket at the bottom labeled 320. The array is also labeled 120 at the top right.

Fig.17

1066	
661	663
PIXEL ID No.	Z VALUE
1	
2	
3	
⋮	⋮

09751393-122700

09/11/93 - 122700

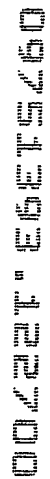
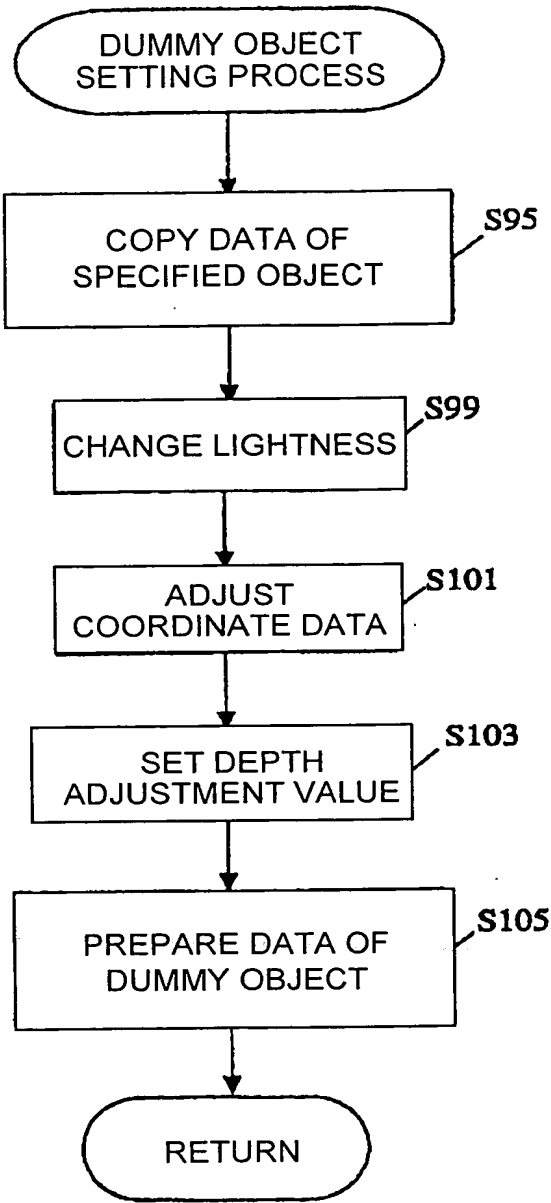
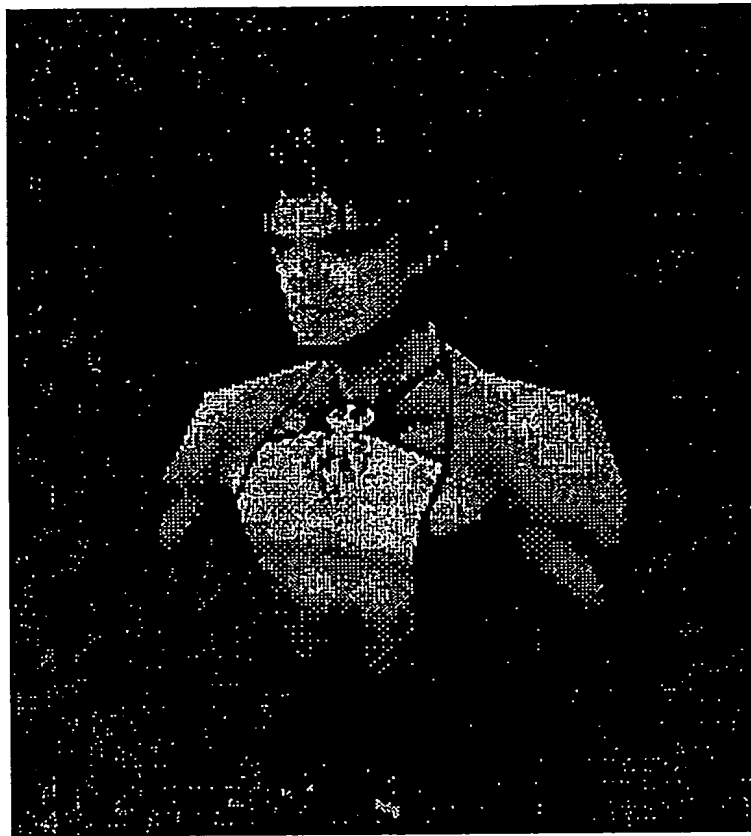


Fig.19



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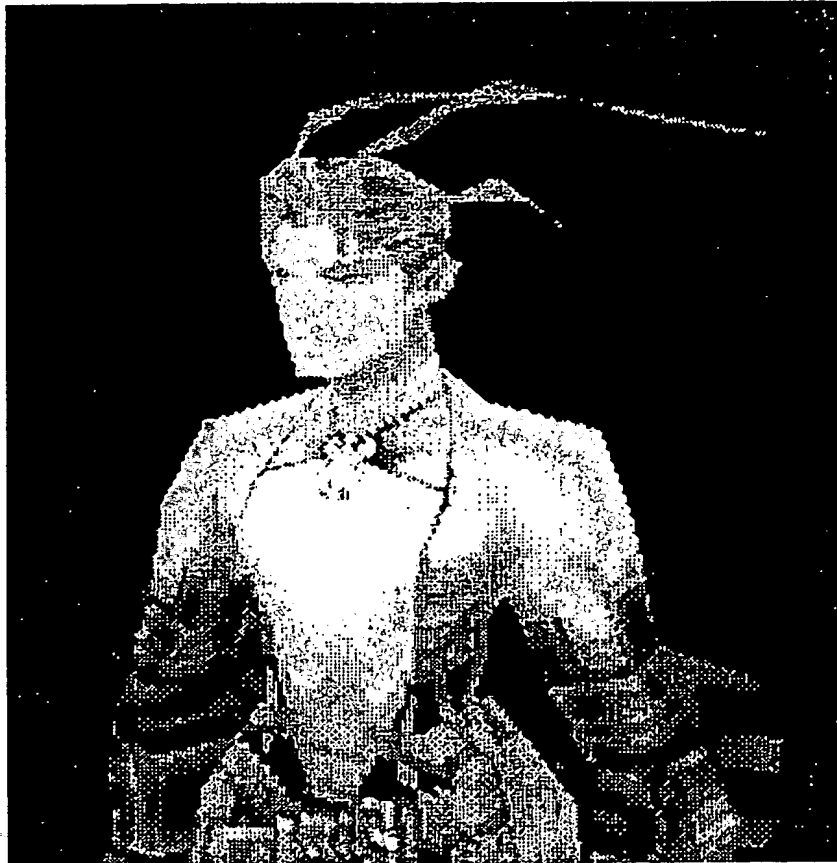
Fig.20



120

09751393 122700

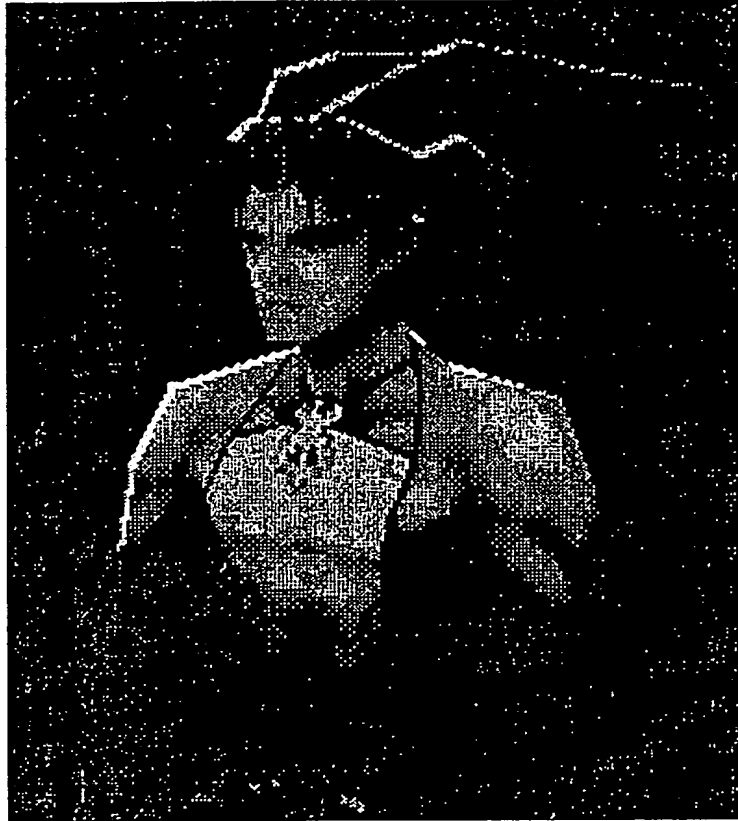
Fig.21



120

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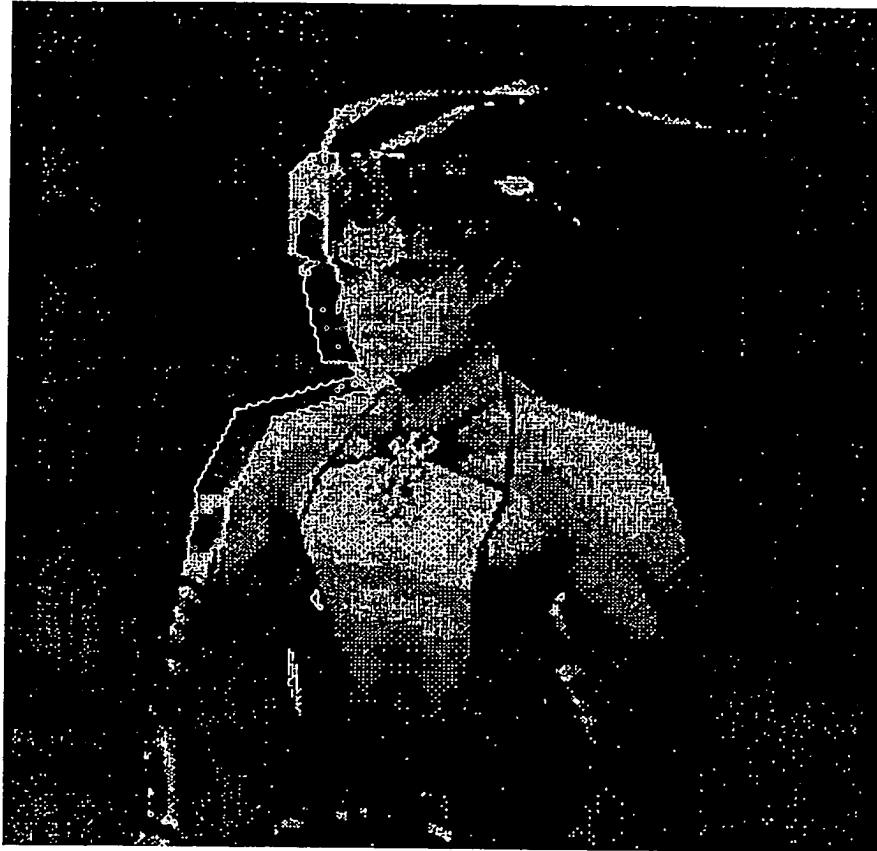
Fig.22



120

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Fig.23



120

00222T E66T5260